INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EXPOSED TERMINALS

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of U.S. Patent application entitled "INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EMBEDDED CONDUCTIVE PATTERNS AND METHOD THEREFOR", serial number 10/138,225 filed May 1, 2002, having at least one common inventor and assigned to the same assignee.

The present application is also a continuation-in-part of U.S. Patent application entitled "INTEGRATED CIRCUIT SUBSTRATE HAVING EMBEDDED BACK-SIDE ACCESS CONDUCTORS AND VIAS", serial number 10/392,737 filed March 19, 2003, by the same inventors and assigned to the same assignee. The specifications of the above-referenced patent applications are herein incorporated by reference.

FIELD OF THE INVENTION

The present invention relates generally to semiconductor packaging, and more specifically, to a substrate having laser ablated terminals for conductors for providing an electrical interface between a die and external terminals in an integrated circuit package.

BACKGROUND OF THE INVENTION

Semiconductors and other electronic and opto-electronic assemblies are fabricated in groups on a wafer. Known as "dies", the individual devices are cut from the wafer and are then bonded to a carrier. The dies must be mechanically mounted and electrically connected to a circuit.

The above-incorporated patent application "INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EMBEDDED CONDUCTIVE PATTERNS AND METHOD THEREFOR" provides increased conductor density and decreased inter-conductor spacing via laser-embedded circuit technologies, but still has a terminal pitch limitation dictated by traditional masking techniques (if any are used) for masking the wirebond points and ball/land grid array terminal mounting points of the exposed copper at the surfaces of the substrate.

The above-incorporated patent application "INTEGRATED CIRCUIT SUBSTRATE HAVING EMBEDDED BACK-SIDE ACCESS CONDUCTORS AND VIAS" provides increased conductor density and lower manufacturing cost by using a prefabricated substrate having metal plated, printed or etched on a dielectric. However, a solder mask is required to prevent plating of the ball/land grid array terminals during the plating process, adding an additional step to the overall manufacturing process. Additionally, other techniques commonly in use for selectively plating wire bonding areas with a Ni/Au or other plating material commonly use a

resist process to mask off the ball/land grid array terminals that would otherwise be exposed after the substrate has been drilled or punched.

Therefore, it would be desirable to provide methods and substrates having improved interconnect density with a low associated manufacturing cost. It would further be desirable to provide a method and substrate wherein external terminals of a substrate may be selectively plated without requiring a masking or resist process.

SUMMARY OF THE INVENTION

The above objectives of providing improved interconnect density and a low associated manufacturing cost and providing improvements in selectively plating terminals without a masking or resist process are provided in a substrate and method for manufacturing a substrate. Laser-ablation is used to remove a coating or drill holes through a substrate to expose the terminals after plating and other manufacturing procedures have been completed.

Unplated terminals may be generated on a dielectric film having a laminated metal layer by imaging and etching the metal layer and then dip-plating without the use of any plating resistive material. The terminals are laser-exposed by ablating

the film from the back-side of the metal layer to form terminal connection points.

Alternatively, a metal layer may be coated with a dielectric material on one or both sides and laser-embedded conductors placed in the dielectric layers and covered with a conformal coating. Wirebond and/or ball/land grid array terminals are laser-exposed by ablating the conformal coating only above the terminals, providing a protected surface having only the terminal locations exposed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1H are pictorial diagrams depicting a cross-sectional view of stages of preparation of an integrated circuit substrate in accordance with an embodiment of the present invention;

Figures 2A and 2B are pictorial diagrams depicting integrated circuits in accordance with embodiments of the present invention;

Figures 3A-3G are a pictorial diagrams depicting a cross-sectional view of stages of preparation of an integrated circuit substrate in accordance with another embodiment of the present invention; and

Figures 4A and 4B are pictorial diagrams depicting integrated circuits in accordance with other embodiments of the present invention.

The invention, as well as a preferred mode of use and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein like reference numerals indicate like parts throughout.

DETAILED DESCRIPTION

Referring now to the figures and in particular to Figure 1A through 1H, a cross-sectional view of stages of preparation of a substrate in accordance with an embodiment of the present invention is shown. A first substrate stage 10A, having a dielectric layer 12 and an adhesive layer 14 disposed thereon is punched to add sprocket holes 16 forming substrate stage 10B of Figure 1B. Sprocket holes 16 are added for machine feeding the substrate stages, which are generally formed on a continuous tape, through processing machines for performing the method that prepares the substrate of the present embodiment. Substrate stage 10A may be fabricated from a dielectric film tape such as a polyimide film. Alternatively, substrate stage 10A may be fabricated from a rigid or semi-rigid dielectric material such as polyimide resin having, in accordance with another embodiment

of the present invention. Suitable tape materials are KAPTON, APICAL, UPILEX and various liquid crystal polymers (LCPs) may also be used to form the core of the substrate of the present invention. Rigid substrate layers may be cured epoxy resin, FR4, or other substrate materials commonly used to form integrated circuit substrates.

Next, a metal conductive layer 18 (generally a copper film) is laminated to substrate stage 10B, using adhesive layer 14 to secure the lamination forming substrate stage 10C of Figure 1C. Substrate 10C is imaged and etched for form a conductive pattern 18A yielding substrate stage 10D of Figure 1D. Substrate state 1D is then immersion plated to deposit a plating forming plated conductive pattern 18B (generally Ni/Au) on conductive pattern 18A yielding substrate stage 10E of Figure 1E. Unique to the method and structure of substrate stage 10E is that no masking is required to selectively plate conductive pattern, which is done for environmental protection and to yield wire-bondable contact surfaces on conductive pattern 18B. It is desirable not to plate solder terminal locations, as eventual diffusion of gold into the solder bond weakens the solder bond, causing early failures due to fracture. Because the solder ball terminals for the external contacts of substrate stage 10D have not been exposed, substrate stage 10D can be plated without masking to

yield substrate stage 10E without plating the external contact terminals.

Next, substrate stage 10E is laser-ablated from the back side to expose terminals for solder ball attach through holes 20 yielding substrate stage 10F. Finally, substrate stage 10F is dipped in an organic solderable protectant (OSP) that coats the terminal locations 22, yielding final substrate 10G.

The above-described process yields an advantage over prior solutions that typically punch all voids in dielectric layer 12 when sprocket holes 16 are punched. Then, in order to selectively plate the conductive pattern (without plating the solder ball terminals) a plating mask is applied through the solder ball terminal holes. The method of the present invention and the consequent resulting structure, provides an advantage of eliminating the masking step in order to produce substrate 1G without gold present in the terminal/solder interfaces.

Referring now to Figure 2A, an integrated circuit 21A, in accordance with an embodiment of the invention is shown. A die 26 is mounted on substrate 10G via a plurality of solder balls or posts 24 in a flip-chip configuration. External terminal solder balls 22 are added to the external terminal locations forming a complete integrated circuit package that may be subsequently encapsulated.

Referring now to Figure 2B, another integrated circuit 21B is shown exemplifying a wire bonded configuration. A die 26A is mounted to substrate 10H with an adhesive (generally epoxy) and wires 24A are bonded between plated lands on the conductive pattern side of substrate 10H. Solder balls 22 are added to the external terminal locations. Substrate 10H is manufactured according to the same steps as substrate 10G, but has a different circuit pattern and die mounting area for accommodating wire-attach type die 26A.

Referring now to Figures 3A-3G, stages of preparation of a substrate in accordance with another embodiment of the invention are shown. A first stage of preparation of substrate 30A is shown as a metal layer 32, which is etched to provide holes 34. Metal layer 32 is generally a copper core that may be etched or die-cut, but other suitable metal layers may be used for form the core of the substrate of the present invention, such as a copper-INVAR-copper laminate. The ratio of copper to Invar can be varied to provide adjustment of the coefficient of thermal expansion (CTE) of the substrate. Holes 34 are generated in metal layer 32 to permit the passage of circuit paths through metal layer 320, while avoiding electrical contact with metal layer 32. Referring now to figure 3B, the second stage of preparation forming substrate stage 30B is shown. A dielectric outer layer 36 has been added to the top and bottom surface of

metal layer 32 and can be provided by injection molding a plastic material around metal layer 32 or by laminating a dielectric such as KAPTON film or PTFE on each side of metal layer 32.

Referring now to Figure 3C, the next stage is depicted. Substrate 30B is laser-ablated to form substrate 30C having vias 38, blind vias 40 and conductor channels 42. Blind vias 40 show a conical shape, which is preferred for addition of conductive material and can be generated by varying the laser angle or beam diameter as dielectric material 36 is ablated.

Next, referring to Figure 3D, the next step in the preparation of substrate 30C providing a substrate 30D having conductive circuit paths. Conductive material is added within channels 42, blind vias 40 and through vias 38 to provide conductive paths 42A conductive blind vias 40A and conductive through vias 38A. The conductive material may be a silver or copper paste that is screen printed into channels 42, blind vias 40 and through vias 38, and planarized to remove conductive material on the surface of outer dielectric layer 36 after printing. Alternatively, an electroplating process (generally copper electroplate) can be used to add conductive material within channels 42, blind vias 40 and through vias 38 and a planarization process or chemical etching process can be used to

remove excess conductive material on the surface of dielectric layer 36.

Next, a conformal coating 44 is applied to both sides of substrate state 30D and cured, yielding coated substrate stage 30E. Then, only terminal areas (wire bond lands and solder ball lands) are laser-ablated in conformal coating 44 to expose the terminal connection areas for solder ball and wire-bond lands 46. Next, plating 48 is applied to the exposed terminals (generally Ni/Au) to provide wire-bondable and solderable surfaces for attachment of wires and/or solder balls forming final substrate 30G.

Nickel-Gold is generally used to provide a barrier migration layer and to provide electrical contact for wire or chip bonding in subsequent manufacturing steps. In general, silver-nickel is an appropriate electroplating material and if a silver paste was used to form conductive channels 42A, blind vias 40A and through vias 38A, plating may not be needed to provide solderable conductive connections, but may be added to eliminate oxidation.

Referring now to Figure 4A, an integrated circuit 21A, in accordance with an embodiment of the invention is shown. A die 26 is mounted on substrate 30G via a plurality of solder balls or posts 24 in a flip-chip configuration. External terminal solder balls 22 are added to the external terminal locations

forming a complete integrated circuit package that may be subsequently encapsulated.

Referring now to Figure 4B, another integrated circuit 41B is shown exemplifying a wire bonded configuration. Die 26A is mounted to substrate 30H with an adhesive (generally epoxy) and wires 24A are bonded between plated lands on the conductive pattern side of substrate 30H. Solder balls 22 are added to the external terminal locations. Substrate 30H is manufactured according to the same steps as substrate 30G, but has a different circuit pattern and die mounting area for accommodating wire-attach type die 26A.

The above description of embodiments of the invention is intended to be illustrative and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the above disclosure and fall within the scope of the present invention.